Refine Search

Search Results -

Terms	Documents
command same "destination address" same "destination data"	37

Database:
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Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, August 09, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	command same "destination address" same "destination data"	37	L3
L2	command same address same data	47567	L2
L1	(MSR adj1 command)	5	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
command same "destination address" same "destination data"	3

Database:
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Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, August 09, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
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L4	command same "destination address" same "destination data"	3	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	command same "destination address" same "destination data"	37	L3
L2	command same address same data	47567	L2
L1	(MSR adj1 command)	5	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
command same "destination address" same "destination data"	3

Database:
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US Patents Full-Text Database
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JPO Abstracts Database
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Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

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Set Name side by side	Query	Hit Count	Set Name result set
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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	command same "destination address" same "destination data"	37	L3
L2	command same address same data	47567	L2
L1	(MSR adj1 command)	5	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3 and (access$3 near5 request)	11

Database:
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JPO Abstracts Database
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Search: L6

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, August 09, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
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L5	l3 same (access near5 request)	0	L5
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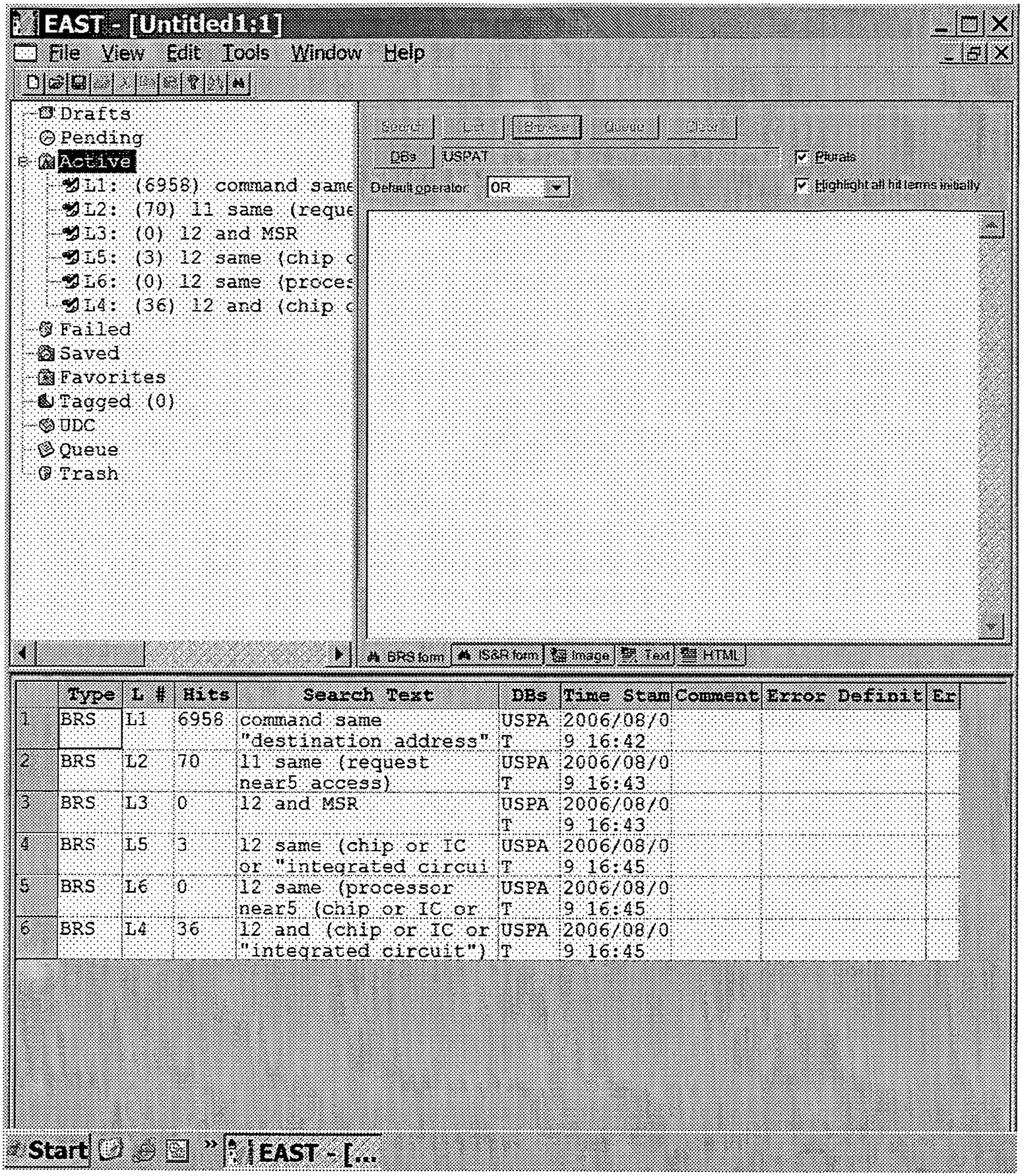
L4	command same "destination address" same "destination data"	3	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	command same "destination address" same "destination data"	37	L3
L2	command same address same data	47567	L2
L1	(MSR adj1 command)	5	L1

END OF SEARCH HISTORY



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2	BRS	L2	70	11 same (request near5 access)	USPAT	2006/08/09 16:43			
3	BRS	L3	0	12 and MSR	USPAT	2006/08/09 16:43			
4	BRS	L5	3	12 same (chip or IC or "integrated circui	USPAT	2006/08/09 16:45			
5	BRS	L6	0	12 same (processor near5 (chip or IC or	USPAT	2006/08/09 16:45			
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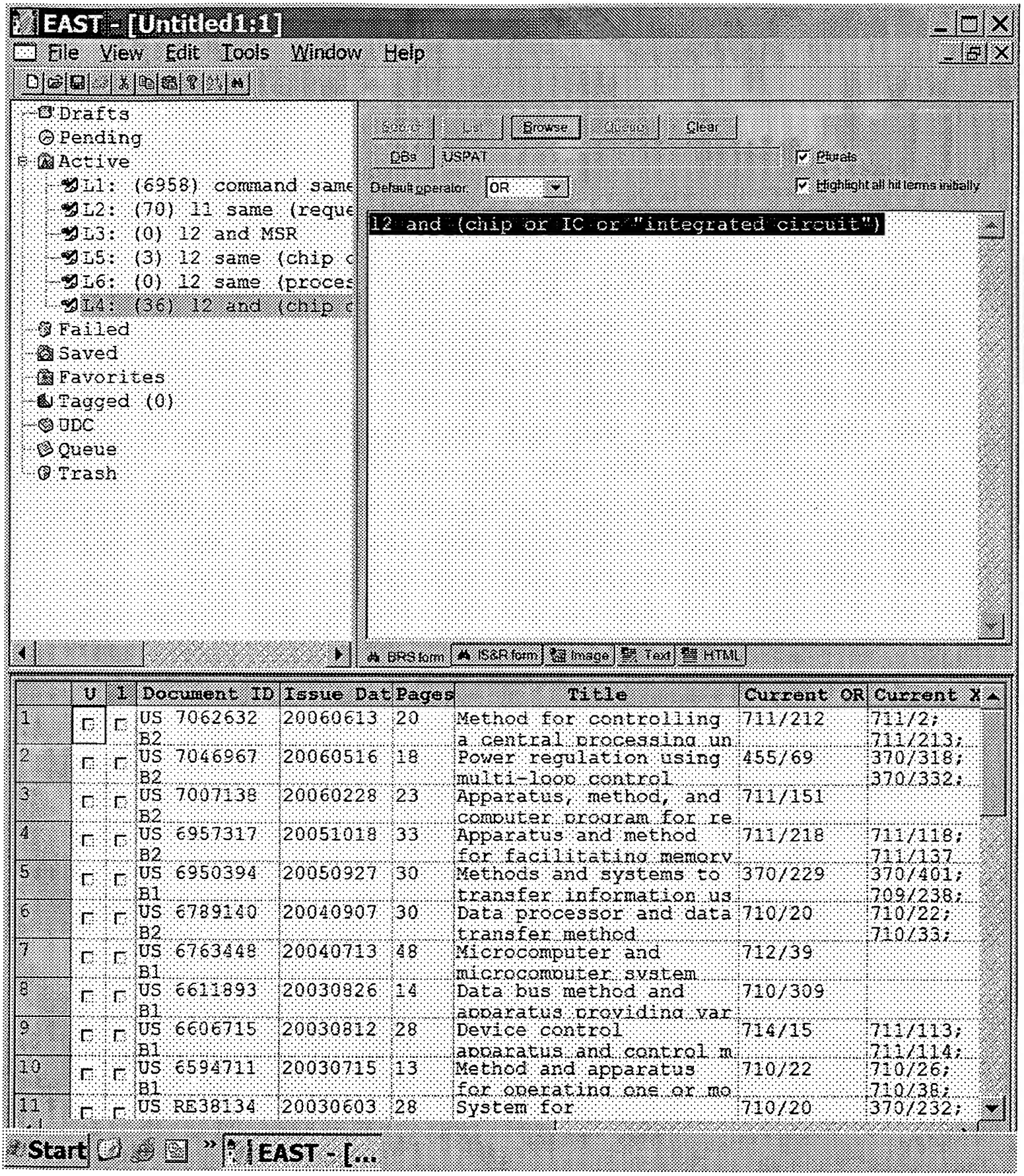
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1 US 7062632 B2 20060613 20 Method for controlling a central processing un 711/212 711/2; 711/213;
2 US 7046967 B2 20060516 18 Power regulation using multi-loop control 455/69 370/318; 370/332;
3 US 7007138 B2 20060228 23 Apparatus, method, and computer program for re 711/151
4 US 6957317 B2 20051018 33 Apparatus and method for facilitating memory 711/218 711/118; 711/137
5 US 6950394 B1 20050927 30 Methods and systems to transfer information us 370/229 370/401; 709/238;
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7 US 6763448 B1 20040713 48 Microcomputer and microcomputer system 712/39
8 US 6611893 B1 20030826 14 Data bus method and apparatus providing var 710/309
9 US 6606715 B1 20030812 28 Device control apparatus and control m 714/15 711/113; 711/114;
10 US 6594711 B1 20030715 13 Method and apparatus for operating one or mo 710/22 710/26; 710/38;
11 US RE38134 20030603 28 System for 710/20 370/232;
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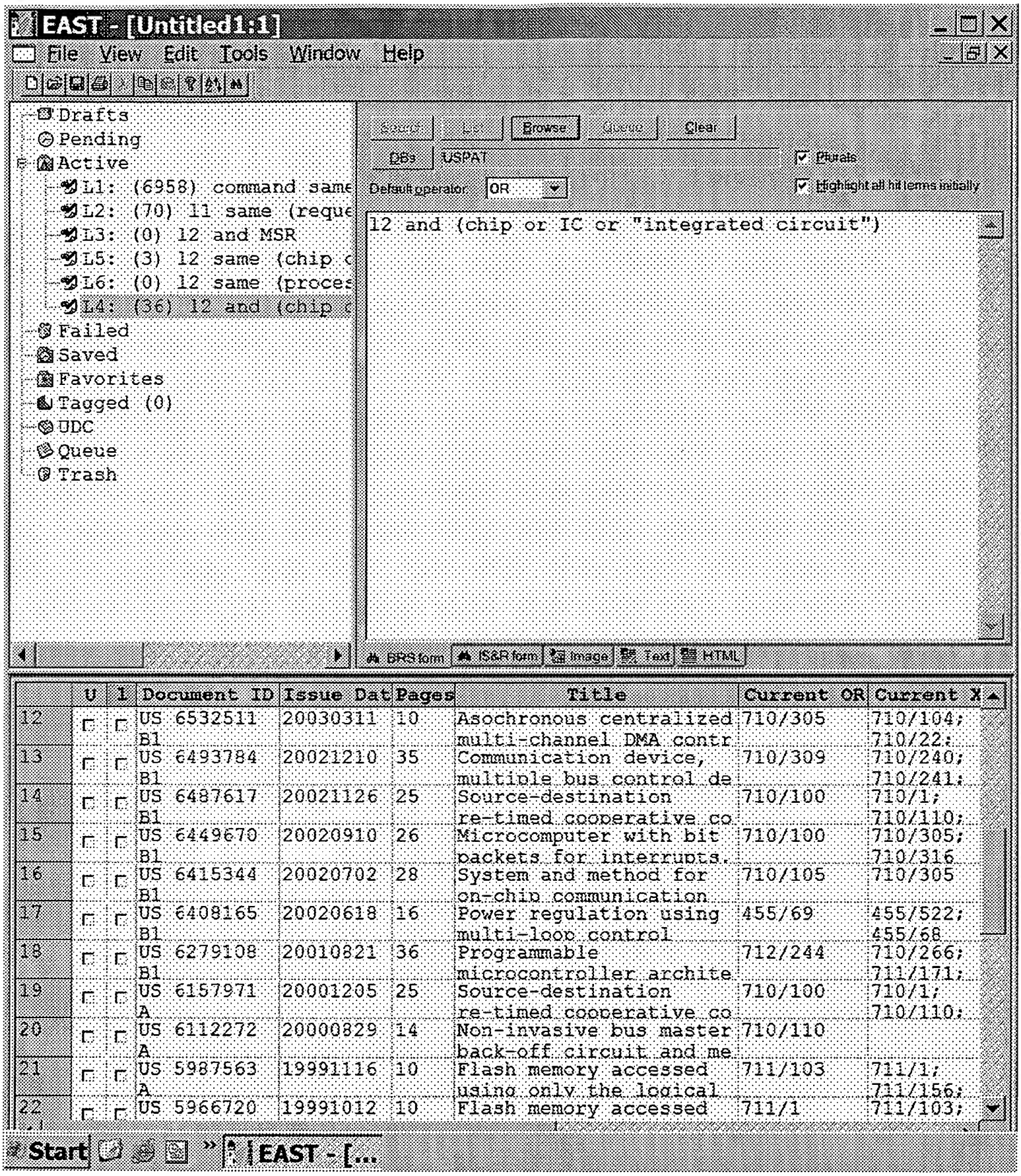

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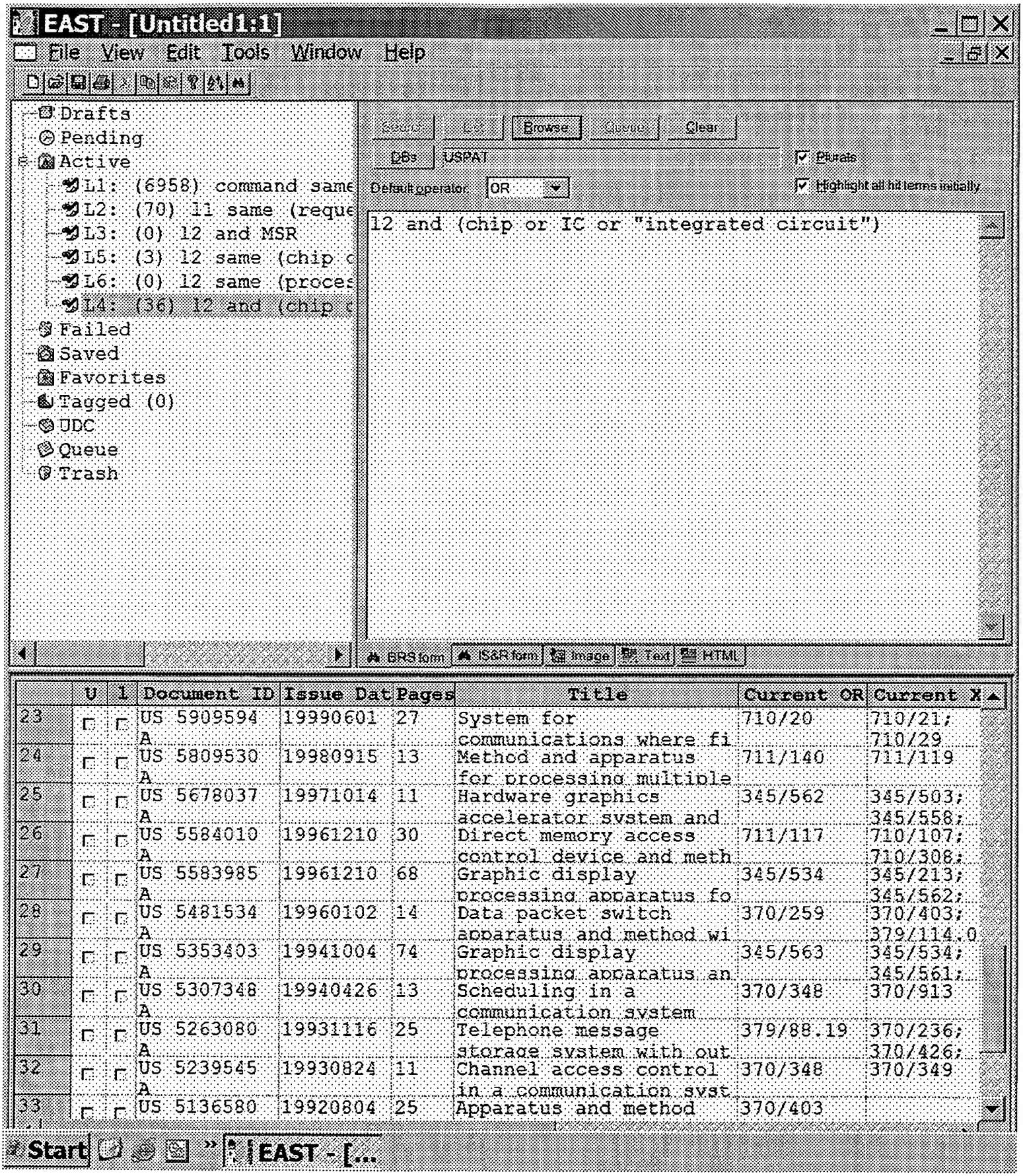
13	☐	☐	US 6493784 B1	20021210	35	Communication device, multiple bus control de	710/309	710/240; 710/241;
14	☐	☐	US 6487617 B1	20021126	25	Source-destination re-timed cooperative co	710/100	710/1; 710/110;
15	☐	☐	US 6449670 B1	20020910	26	Microcomputer with bit packets for interrupts.	710/100	710/305; 710/316
16	☐	☐	US 6415344 B1	20020702	28	System and method for on-chip communication	710/105	710/305
17	☐	☐	US 6408165 B1	20020618	16	Power regulation using multi-loop control	455/69	455/522; 455/68
18	☐	☐	US 6279108 B1	20010821	36	Programmable microcontroller archite	712/244	710/266; 711/171;
19	☐	☐	US 6157971 A	20001205	25	Source-destination re-timed cooperative co	710/100	710/1; 710/110;
20	☐	☐	US 6112272 A	20000829	14	Non-invasive bus master back-off circuit and me	710/110	
21	☐	☐	US 5987563 A	19991116	10	Flash memory accessed using only the logical	711/103	711/1; 711/156;
22	☐	☐	US 5966720	19991012	10	Flash memory accessed	711/1	711/103;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23 US 5909594 A 19990601 27 System for communications where fi 710/20 710/21; 710/29
24 US 5809530 A 19980915 13 Method and apparatus for processing multiple 711/140 711/119
25 US 5678037 A 19971014 11 Hardware graphics accelerator system and 345/562 345/503; 345/558;
26 US 5584010 A 19961210 30 Direct memory access control device and meth 711/117 710/107; 710/308;
27 US 5583985 A 19961210 68 Graphic display processing apparatus fo 345/534 345/213; 345/562;
28 US 5481534 A 19960102 14 Data packet switch apparatus and method wi 370/259 370/403; 379/114.0
29 US 5353403 A 19941004 74 Graphic display processing apparatus an 345/563 345/534; 345/561;
30 US 5307348 A 19940426 13 Scheduling in a communication system 370/348 370/913
31 US 5263080 A 19931116 25 Telephone message storage system with out 379/88.19 370/236; 370/426;
32 US 5239545 A 19930824 11 Channel access control in a communication syst 370/348 370/349
33 US 5136580 19920804 25 Apparatus and method 370/403
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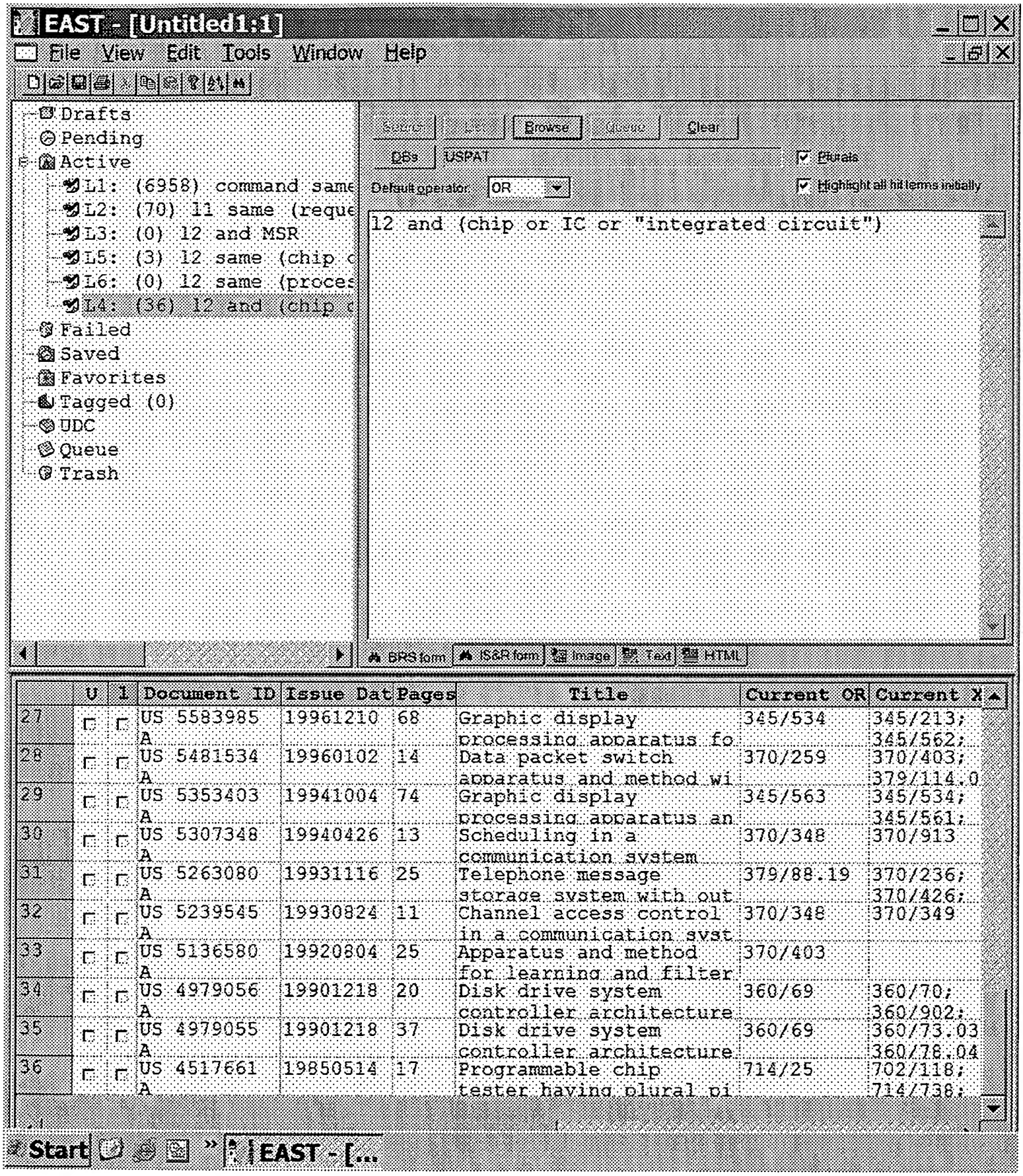
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27 US 5583985 A 19961210 68 Graphic display processing apparatus fo 345/534 345/213; 345/562;
28 US 5481534 A 19960102 14 Data packet switch apparatus and method wi 370/259 370/403; 379/114.0
29 US 5353403 A 19941004 74 Graphic display processing apparatus an 345/563 345/534; 345/561;
30 US 5307348 A 19940426 13 Scheduling in a communication system 370/348 370/913
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32 US 5239545 A 19930824 11 Channel access control in a communication syst 370/348 370/349
33 US 5136580 A 19920804 25 Apparatus and method for learning and filter 370/403
34 US 4979056 A 19901218 20 Disk drive system controller architecture 360/69 360/70; 360/902;
35 US 4979055 A 19901218 37 Disk drive system controller architecture 360/69 360/73.03 360/78.04
36 US 4517661 A 19850514 17 Programmable chip tester having plural pi 714/25 702/118; 714/738;
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IEE JNL	IEE Journal or Magazine
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IEE CNF	IEE Conference Proceeding
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   Kynett, V.; Anderson, J.; Atwood, G.; Dix, P.; Fandrich, M.; Jungroth, O.; Kao, S.; Kreifels, J.A.; Lai, S.; Liou, H.-C.; Liu, B.; Lodenquai, R.; Lu, W.-J.; Pavloff, R.; Tang, D.; Tsau, G.; Tzeng, J.C.; Vajdic, B.; Verma, G.; Wang, S.; Wells, S.; Winston, M.; Yang, L.;
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Hierarchical system test by an IEEE 1149.5 MTM-bus slave-module interface core

Jin-Hua Hong Chung-Hung Tsai Cheng-Wen Wu
Dept. of Electr. Eng., Nat. Tsing Hua Univ., Hsinchu, Taiwan;

This paper appears in: Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Publication Date: Oct. 2000
Volume: 8 , Issue: 5
On page(s): 503 - 516
Meeting Date: 12/02/1998 - 12/04/1998
Location: Hsinchu
ISSN: 1063-8210
CODEN: IEVSE9
INSPEC Accession Number:6830778
Digital Object Identifier: 10.1109/92.894154
Posted online: 2002-08-06 23:32:01.0

Abstract
An IEEE 1149.5 module test and maintenance (MTM) bus slave module interface core is presented, which is used for direct access from the system bus to the IEEE 1149.1 chip-level or on-chip buses to facilitate hierarchical system test and diagnosis. The hierarchical test methodology also is presented, which is applicable to the system-on-chip environment, All the standard 1149.1 instructions, such as SAMPLE/PRELOAD, EXTEST, BYPASS, and even RUNBIST, can be performed within three 1149.5 read/write-**data** message cycles. The messages are transmitted between the MTM-bus master module (III-module) and the slave module (S-module). We adopt the full test access **port** control method to activate the 1149.1 boundary-scan paths via the 1149.5 MTM-bus. Our S-module interface circuit implements 16 CORE **commands** and one read/write-**data** command. It has been prototyped using a field-programmable gate array chip and implemented by a full-custom chip. Hierarchical test of multiple 1149.1 compatible boards has been experimentally verified

Index Terms
Inspec
Controlled Indexing
IEEE standards automatic testing boundary scan testing field programmable gate arrays hierarchical systems logic testing

Non-controlled Indexing
IEEE 1149.5 MTM-bus slave-module interface core boundary-scan paths field-programmable gate array chip full test access **port** control method hierarchical system test module test and maintenance multiple 1149.1 compatible boards read/write-**data** command read/write-**data** message cycles
Author Keywords
Not Available

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